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EXAMINER	
MILLS, DONALD L	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 11/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,019	HIROTA ET AL.	
	Examiner	Art Unit	
	Donald L. Mills	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5 and 7* is/are allowed.

6)☒ Claim(s) *1-4,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3, 4, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujimoto (U.S. patent No. 4,748,623).

Referring to claim 3, Fujimoto discloses *a time-division bit-interleave multiplexing* (time division multiplexing, col. 1 lines 11-22) *method comprising:*

(a) Step of generating a plurality of first signals and a plurality of second signals to which specific pulse trains (pulse train, col. 1 lines 15-25) *for frame synchronization* (frame synchronization, col. 1 line 6 - sol. 2 line 2, col. 5 lines 55-68 and col. 9 lines 15-20) *are allocated respectively;*

(b) A step of generating low speed signals (speed signal, col. 1 lines 60-67) *of plural channels including said first and second signals and transmission signals;*

(c) A step of partly converting (converter, col. 4 lines 55-65 and converted, col. 10 lines 15-25) *said first and second signals in either of each odd channel and each even channel into all "0" signals, while partly converting* (converter, col. 4 lines 55-65 and converted, col. 10 lines 15-25) *said first and second signals in the other channels into all "1" signals; and*

(d) A step of time-division multiplexing (time division multiplexing, col. 1 lines 11-22) *said low speed signals* (speed signal, col. 1 lines 60-67) *after said step (c), thereby producing high-speed signals (high-speed signal, col. 1 lines 65-68).*

Referring to claim 4, Fujimoto discloses *a time-division bit-interleave multiplexing* (time division multiplexing, col. 1 lines 11-22) *method comprising:*

(a) A step of generating a plurality of first signals and a plurality of second signals to which specific pulse trains (pulse train, col. 1 lines 15-25*) for frame synchronization* (frame synchronization, col. 1 line 6 - sol. 2 line 2, col. 5 lines 55-68 and col. 9 lines 15-20) *are allocated respectively;*

(b) A step of generating low speed signals (speed signal, col. 1 lines 60-67) *of plural channels including said first and second signals and transmission signals;*

(c) A step of partly converting (converter, col. 4 lines 55-65 and converted, col. 10 lines 15-25) *said first and second signals in either of each odd channel and each even channel into inverted* (inverting, col. 6 lines 20-25) *signals; and*

(d) A step of time-division multiplexing (time division multiplexing, col. 1 lines 11-22) *said low speed signals* (speed signal, col. 1 lines 60-67) *after said step (c), thereby producing high-speed signals* (high-speed signal, col. 1 lines 65-68).

Referring to claim 8, Fujimoto discloses *a time-division bit-interleave multiplexing* (time division multiplexing, col. 1 lines 11-22) *method comprising:*

(a) A step of generating a plurality of first and a plurality of second signals to which specific pulse trains (pulse train, col. 1 lines 15-25) *for frame synchronization* (frame synchronization, col. 1 line 6 - sol. 2 line 2, col. 5 lines 55-68 and col. 9 lines 15-20) *are allocated respectively;*

(b) A step of generating low speed signals (speed signal, col. 1 lines 60-67) *of plural channels including said first and second signals and transmission signals;*

(c) A step of entirely converting (converter, col. 4 lines 55-65 and converted, col. 10 lines 15-25) *said first and second signals in either of each odd channel and each even channel into inverted* (inverting, col. 6 lines 20-25) *signals; and*

(d) A step of time-division multiplexing (time division multiplexing, col. 1 lines 11-22) *said low speed signals* (speed signal, col. 1 lines 60-67) *after said step (c), thereby producing high-speed signals* (high-speed signal, col. 1 lines 65-68).

4. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Suh et al. (U.S. Patent No. 5,710,774).

Referring to claim 6, Suh et al. discloses *a time-division bit-interleave multiplexing* (time-division multiplexing, col. 1 lines 15-24) *method comprising:*

(a) A step of generating a plurality of first signals and a plurality of second signals to which specific pulse trains (pulse train, col. 1 lines 20-24) *for frame synchronization* (frame synchronization, col. 1 lines 15-52, col. 7 lines 35-45 and col. 9 lines 7-11) *are allocated respectively;*

(b) A step of generating low speed signals (speed signal, col. 1 lines 25-34) *of plural channel including said first and second signals and transmission signals;*

(c) A step of partly converting (converting, col. 2 lines 15-30, col. 6 lines 45-55 and col. 7 lines 1-10) *said first and second signals in either of each odd channel and each even channel into random patterns, while partly converting* (converting, col. 2 lines 15-30, col. 6 lines 45-55 and col. 7 lines 1-10) *said first and second signals in the other channels into inverted* (inverted signal, col. 5 lines 46-60) *random patterns obtained by inverting* (inverted signal, col. 5 lines 46-60) *said random patterns; and*

(d) A step of time-division multiplexing (time-division multiplexing, col. 1 lines 15-24) *said low speed signals after said step (c), thereby producing high-speed signals* (high-speed signal, col. 1 lines 25-34).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (U.S. patent No. 4,748,623).

Referring to claim 1, Fujimoto discloses *a time-division bit-interleave multiplexing* (time division multiplexing, col. 1 lines 11-22) *method comprising:*

(a) A step of generating a plurality of first signals and a plurality of second signals to which specific pulse trains (pulse train, col. 1 lines 15-25) *for frame synchronization* (frame synchronization, col. 1 line 6 - col. 2 line 2, col. 5 lines 55-68 and col. 9 lines 15-20) *are allocated respectively;*

(b) A step of generating low speed signals (speed signal, col. 1 lines 60-67) *of plural channels including said first and second signals and transmission signals;*

(c) A step of partly converting (converter, col. 4 lines 55-65 and converted, col. 10 lines 15-25) *said first and second signals in each channel into either of "1/0" alternating signals, said "1/0" alternating signals being repeated patterns of bits "10", and "0/1" alternating signals, said "0/1" alternating signals being repeated patterns of bits "01"* (Converting ODATA into DATA1-4.); *and*

(d) A step of time-division multiplexing said low speed signals (speed signal, col. 1 lines 60-67) *after said step (c), thereby producing high-speed signals* (high-speed signal, col. 1 lines 65-68).

Fujimoto does not disclose *converting the first and second signals in each channel into either of "1/0" alternating signals, the "1/0" alternating signals being repeated patterns of bits "10", and "0/1" alternating signals, the "0/1" alternating signals being repeated patterns of bits "01".*

Fujimoto teaches a frame synchronization circuit comprising a signal separation circuit **1** which separates a high order digital multiplexed input signal into a predetermined number of signal trains using series-to-parallel conversion via an arbitrary frame synchronizing pattern of specified length (See column 3, lines 49-62; column 10, lines 38-40 and 66-67; and column 11, lines 1-4.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the frame synchronization pattern of Fujimoto as alternating "10" and "01" patterns. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to increase system efficiency and reduce pseudo-synchronization by increasing bit-pattern variation, as taught by Fujimoto as being within the scope of the prior art (See column 10, lines 66-67 and column 11, lines 1-4.)

Referring to claim 2, Fujimoto discloses *a time-division bit-interleave multiplexing* (time division multiplexing, col. 1 lines 11-22) *method comprising:*

(a) A step of generating a plurality of first signals and a plurality of second signals to which specific pulse trains (pulse train, col. 1 lines 15-25) *for frame synchronization* (frame synchronization, col. 1 line 6 - sol. 2 line 2, col. 5 lines 55-68 and col. 9 lines 15-20) *are allocated respectively;*

(b) A step of generating low speed (speed signal, col. 1 lines 60-67*) signals of plural channels including said first and second signals and transmission signals;*

(c) A step of partly converting (converter, col. 4 lines 55-65 and converted, col. 10 lines 15-25) *said first and second signals in either of each odd channel and each even channel into "1/0" alternating signals* (converter, col. 4 lines 55- 65 and converted, col. 10 lines 15-25) *said first and second signals in the other channels into "0/1" alternating signals; and*

(d) A step of time-division multiplexing (time division multiplexing, col. 1 lines 11-22) said low speed signals (speed signal, col. 1 lines 60-67) *after said step (c), thereby producing high-speed signals* (high-speed signal, col. 1 lines 65-68).

Fujimoto does not disclose *converting the first and second signals in each channel into either of "1/0" alternating signals, the "1/0" alternating signals being repeated patterns of bits "10", and "0/1" alternating signals, the "0/1" alternating signals being repeated patterns of bits "01".*

Fujimoto teaches a frame synchronization circuit comprising a signal separation circuit **1** which separates a high order digital multiplexed input signal into a predetermined number of signal trains using series-to-parallel conversion utilizing an arbitrary frame synchronizing pattern of specified length (See column 3, lines 49-62; column 10, lines 38-40 and 66-67; and column 11, lines 1-4.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the frame synchronization pattern of Fujimoto as alternating "10" and "01" patterns. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to increase system efficiency and reduce pseudo-synchronization by increasing

bit-pattern variation, as taught by Fujimoto as being within the scope of the prior art (See column 10, lines 66-67 and column 11, lines 1-4.)

Allowable Subject Matter

7. Claims 5 and 7 are allowed.

Response to Arguments

8. Applicant's arguments with respect to claims 1 and 2 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's arguments filed 27 April 2006 have been fully considered but they are not persuasive with regards to claims 3, 4, 6, and 8.

Rejection Under 35 USC 102

On page 9 of the remarks, regarding claim 3, the Applicant argues Fujimoto does not disclose *partly converting the first and second signals in either of each odd channel and each even channel into all "0" signals, while partly converting the first and second signals in the other channels into all "1" signals.* The Examiner respectfully disagrees. Fujimoto teaches, as seen in Figure 5, partially converting the ODATA frame synchronization pattern into "0" bit values in DATA1 and "1" bit values in DATA2. Therefore, Fujimoto discloses *partly converting the first and second signals in either of each odd channel and each even channel into all "0" signals, while partly converting the first and second signals in the other channels into all "1" signals.*

On page 10 of the remarks, regarding claims 4 and 8, the Applicant argues, "a clock signal is not a data signal." The Examiner respectfully agrees, however, "a data signal" is not claimed.

On page 12 of the remarks, regarding claim 6, the Applicant argues Suh does not disclose the *step of partly converting said first and second signals in either of each odd channel and each even channel into random patterns, while partly converting said first and second signals in the other channels into inverted random patterns obtained by inverting said random patterns.* The Examiner respectfully disagrees. Suh discloses when the first frame alignment bytes in a certain frame at the overhead interval are inputted in serial, the input data signal is converted into the 8-bits of parallel data S1 to S8 by the converting circuit **10** depending on the input of the reference clock (See column 7, lines 1-10.) Therefore, Suh discloses *step of partly converting said first and second signals in either of each odd channel and each even channel into random patterns, while partly converting said first and second signals in the other channels into inverted random patterns obtained by inverting said random patterns.*

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald L. Mills whose telephone number is 571-272-3094. The examiner can normally be reached on 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donald L Mills
DLM
November 12, 2006

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